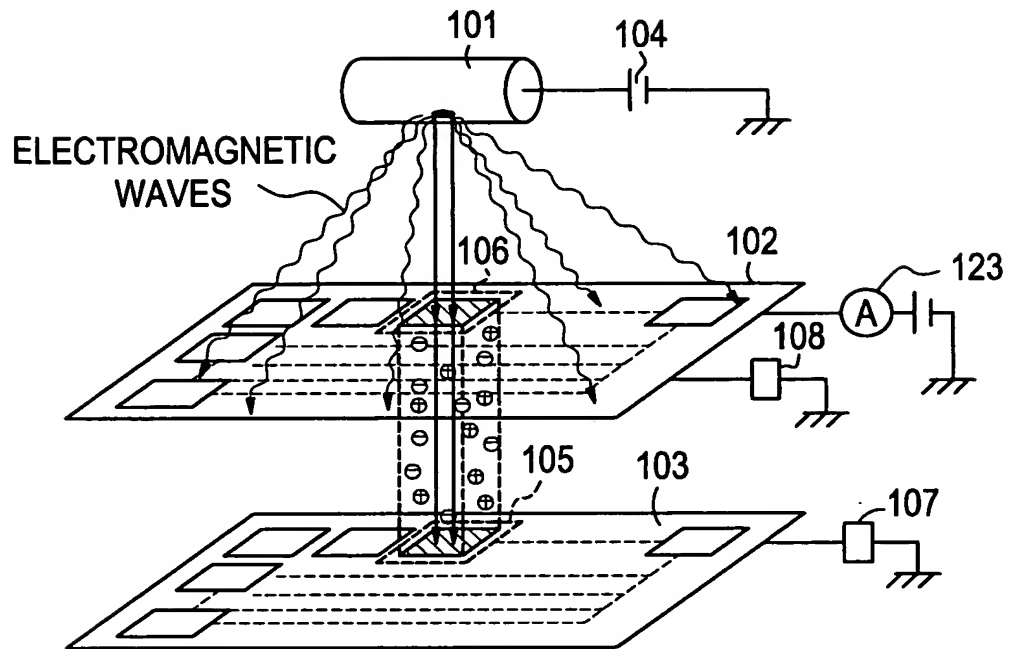
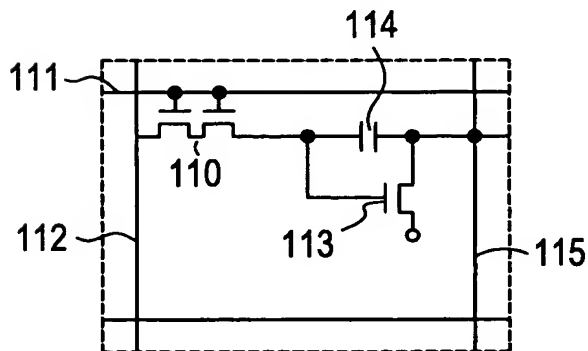


FIG. 1A**FIG. 1B**

ENLARGED DIAGRAM OF 105

**FIG. 1C**

ENLARGED DIAGRAM OF 106

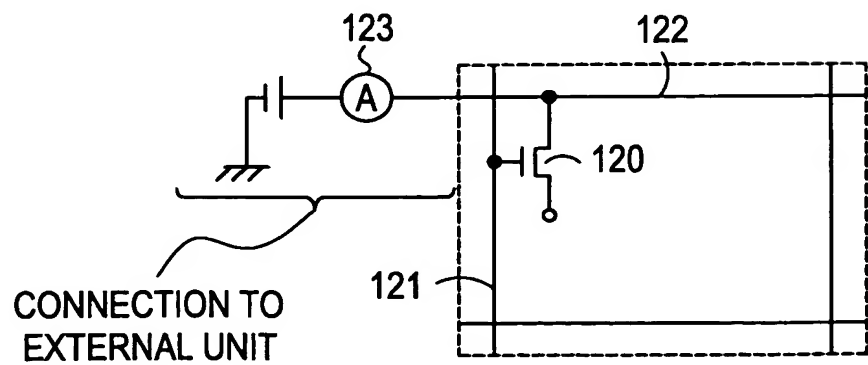


FIG. 2A

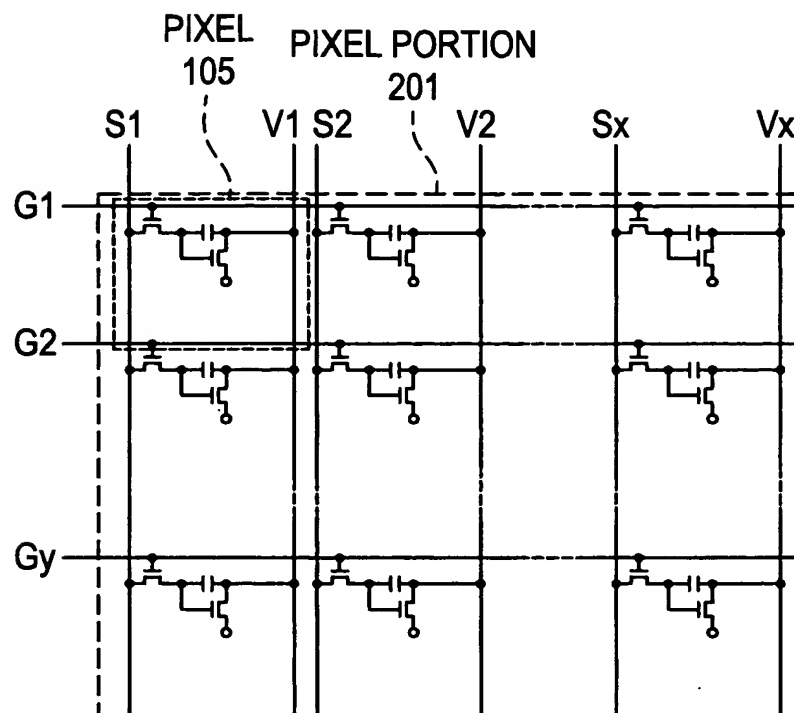


FIG. 2B

OPPOSING PORTION

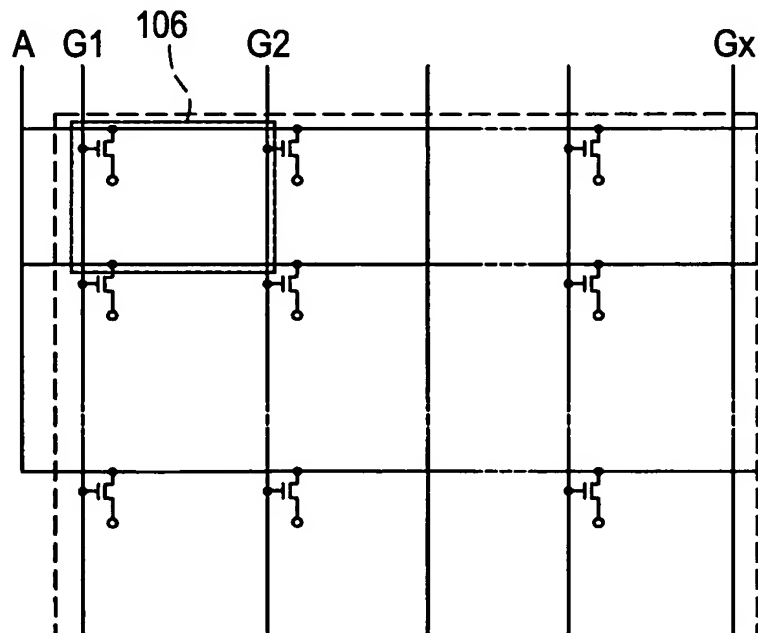


FIG. 3A

(1, 1)	(2, 1)	(3, 1)	(4, 1)		(x-1, 1)	(x, 1)
(1, 2)	(2, 2)	(3, 2)	(4, 2)		(x-1, 2)	(x, 2)
(1, 3)	(2, 3)	(3, 3)	(4, 3)		(x-1, 3)	(x, 3)
(1, 4)	(2, 4)	(3, 4)	(4, 4)		(x-1, 4)	(x, 4)
(1, y-1)	(2, y-1)	(3, y-1)	(4, y-1)		(x-1, y-1)	(x, y-1)
(1, y)	(2, y)	(3, y)	(4, y)		(x-1, y)	(x, y)

FIG. 3B

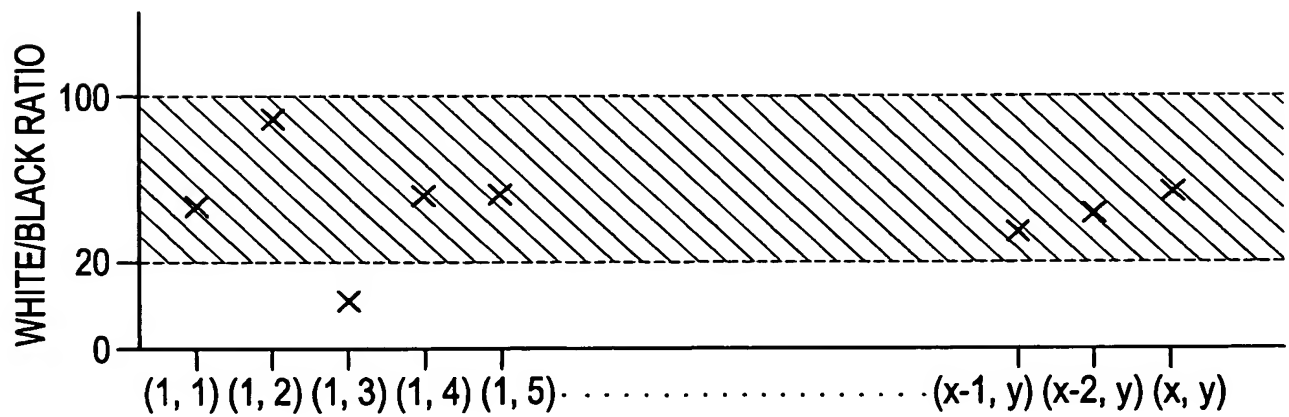


FIG. 4A

FORMATION OF ISLAND SEMICONDUCTOR LAYER, GATE-INSULATING FILM,
AND FIRST AND SECOND CONDUCTING FILMS FOR GATE ELECTRODES

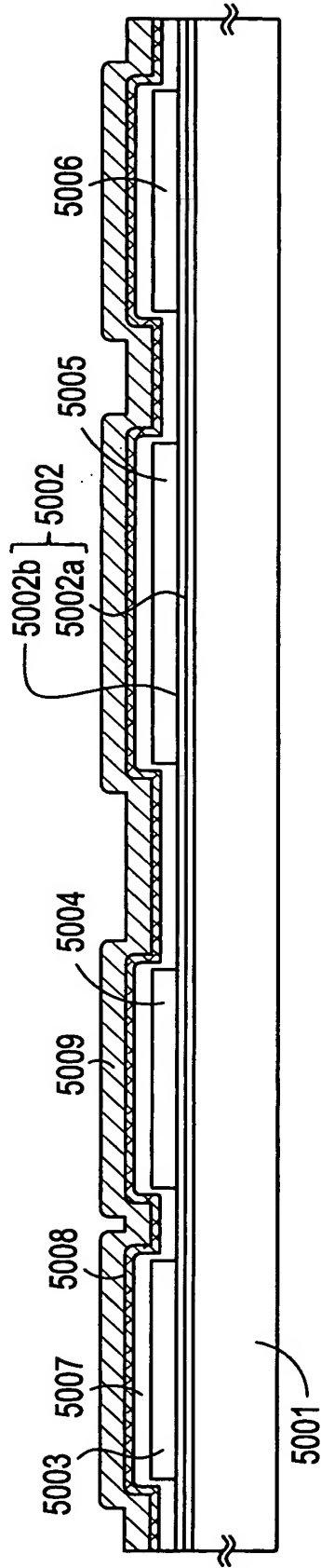


FIG. 4B

FIRST ETCHING AND FIRST DOPING

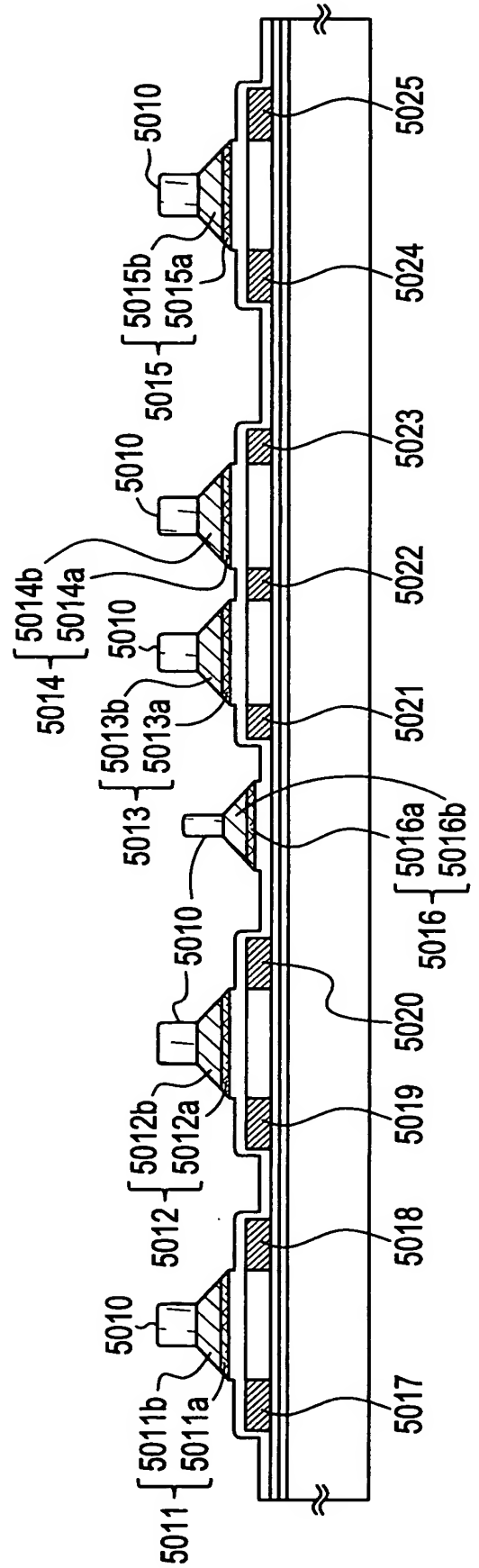


FIG. 4C
SECOND ETCHING

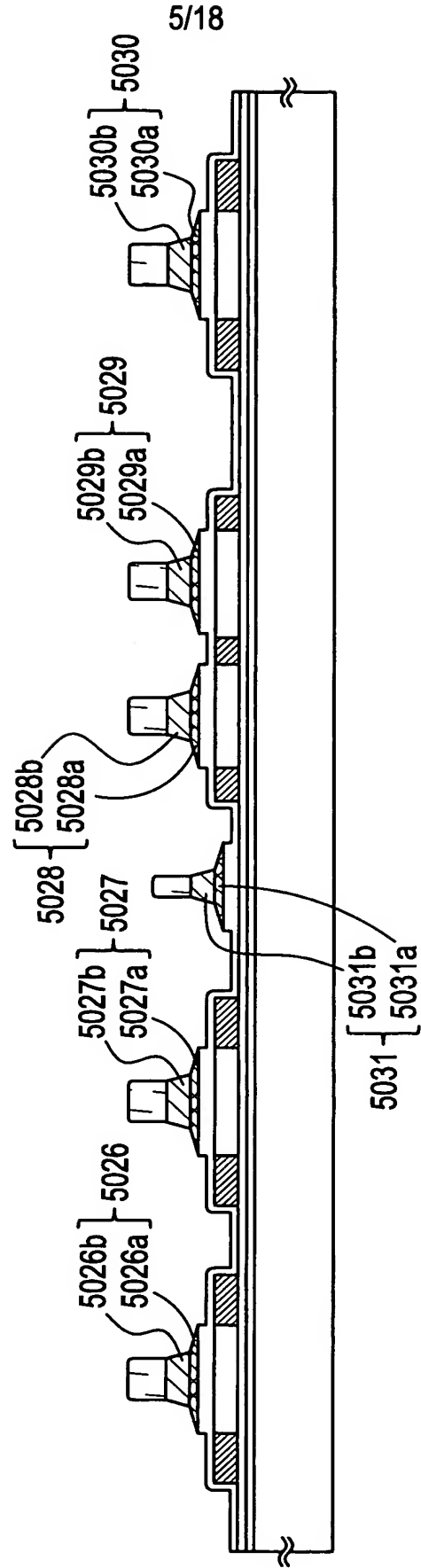


FIG. 5A
SECOND DOPING

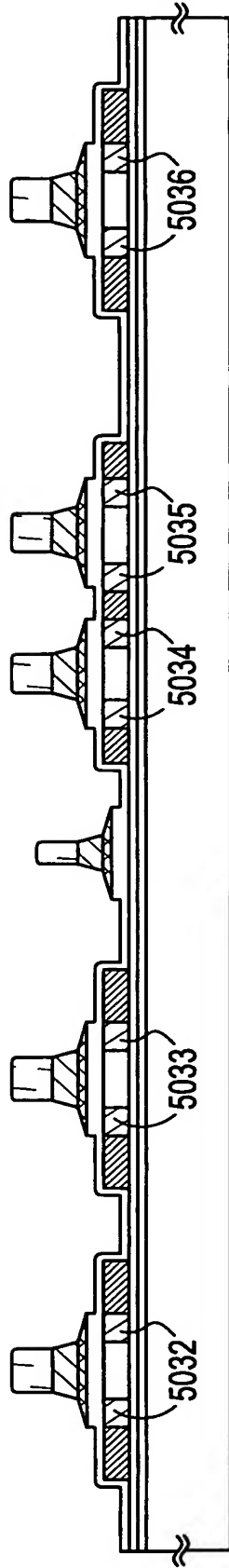


FIG. 5B
THIRD ETCHING

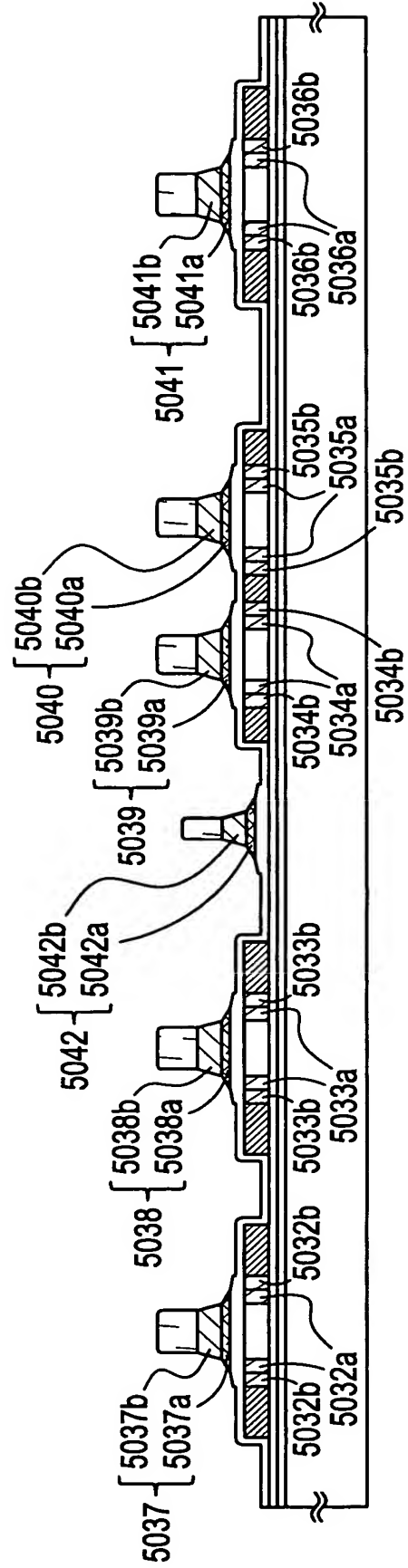


FIG. 5C
THIRD DOPING

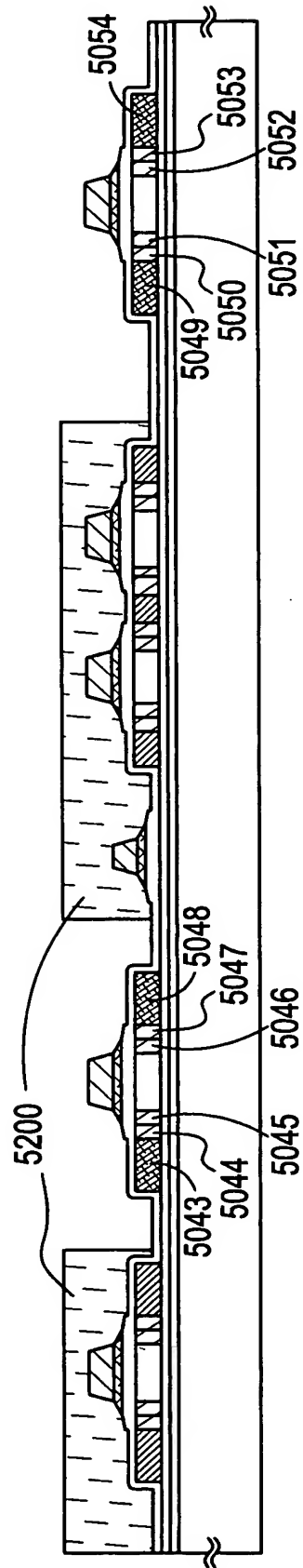


FIG. 6A

FORMATION OF THE FIRST AND SECOND INTERLAYER-INSULATING FILMS, WIRINGS AND PIXEL ELECTRODES

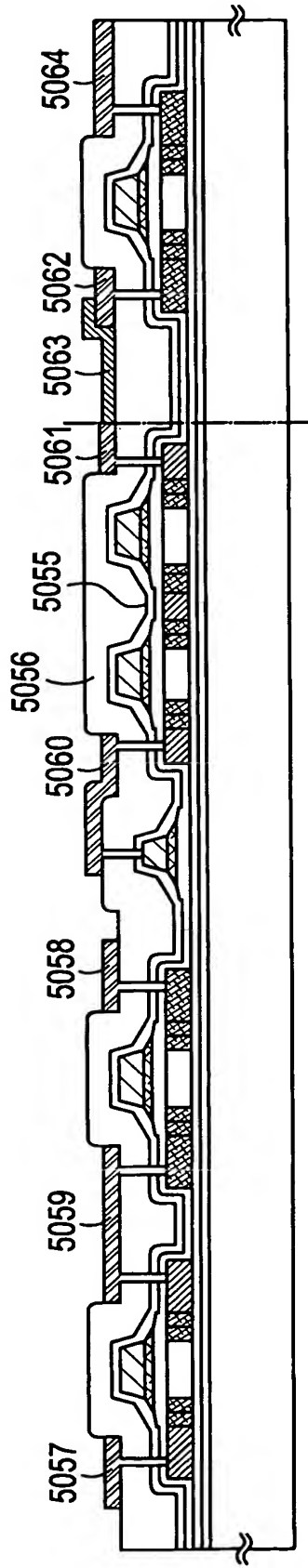


FIG. 6B

FORMATION OF THE THIRD INTERLAYER-INSULATING FILM, EL LAYER, CATHODES AND PASSIVATION FILM

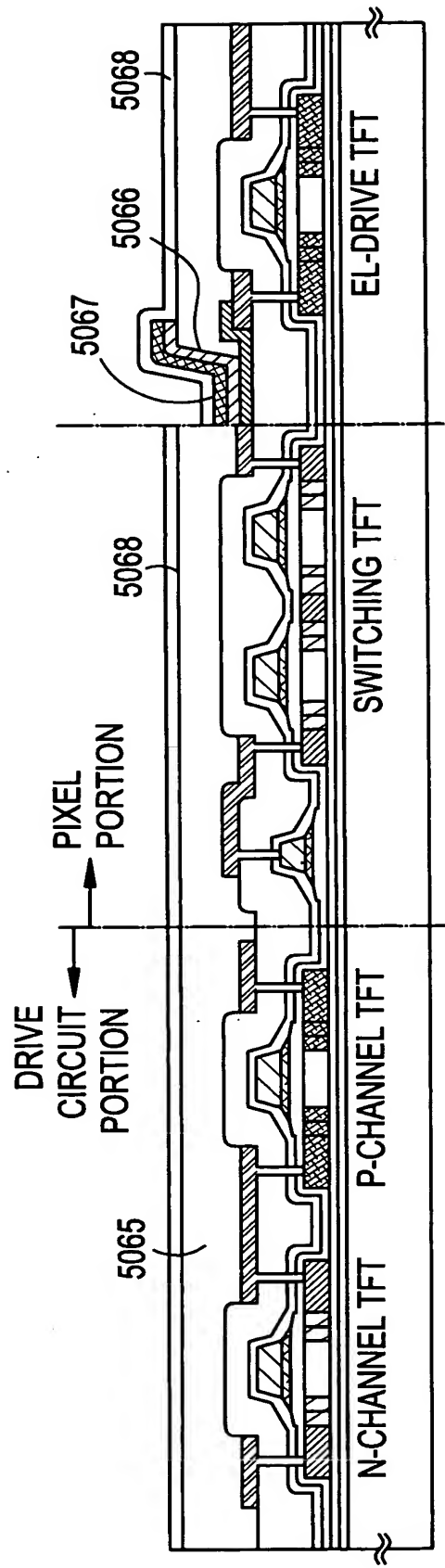


FIG. 7A

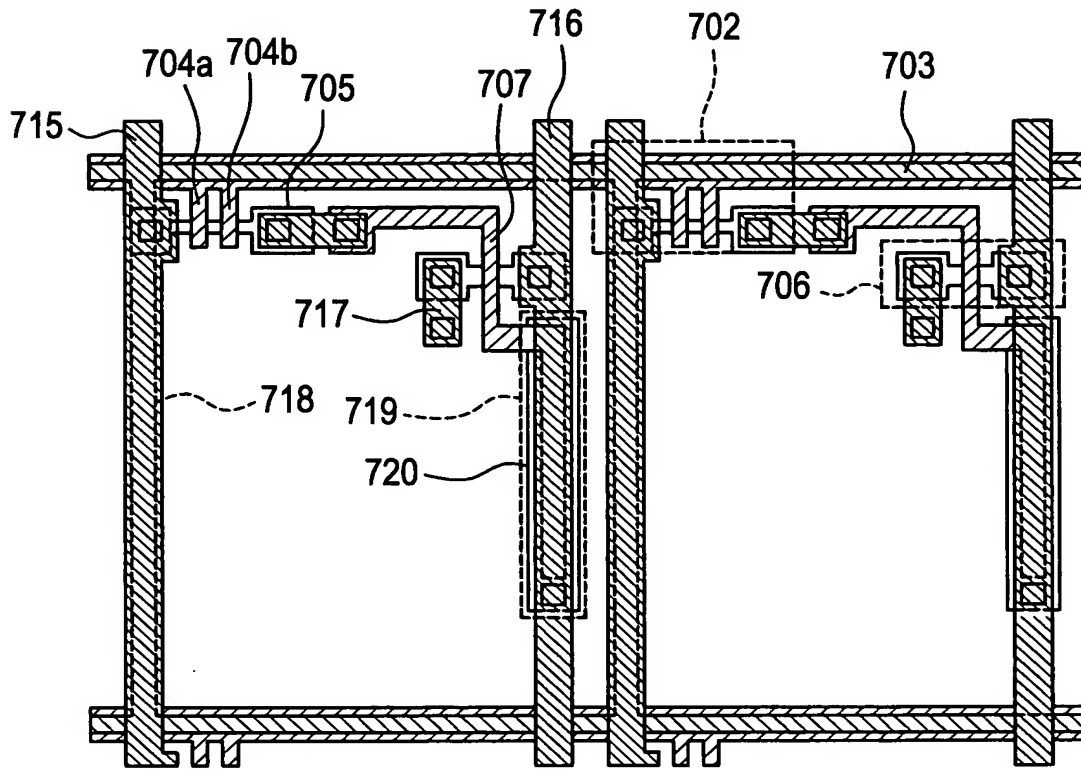


FIG. 7B

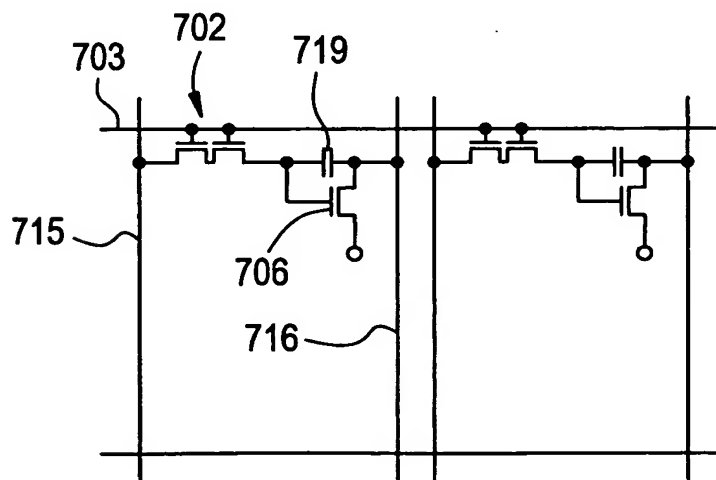


FIG. 8A

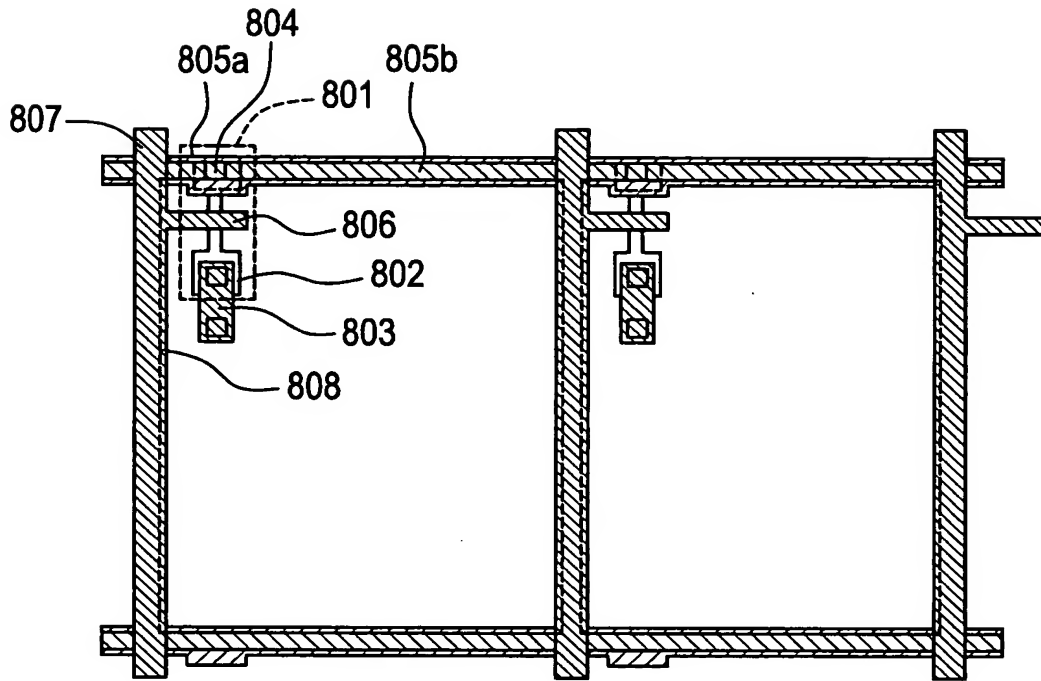


FIG. 8B

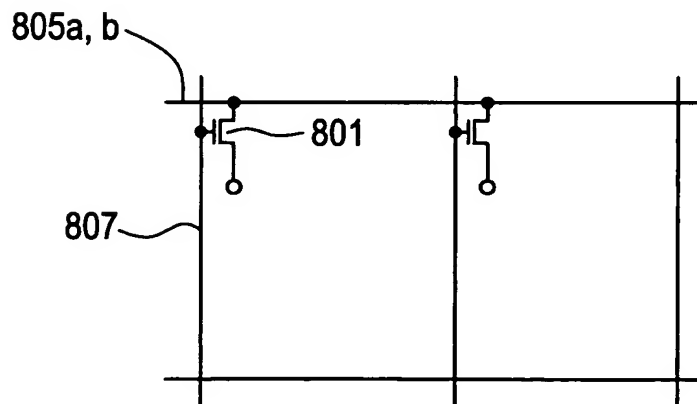


FIG. 9

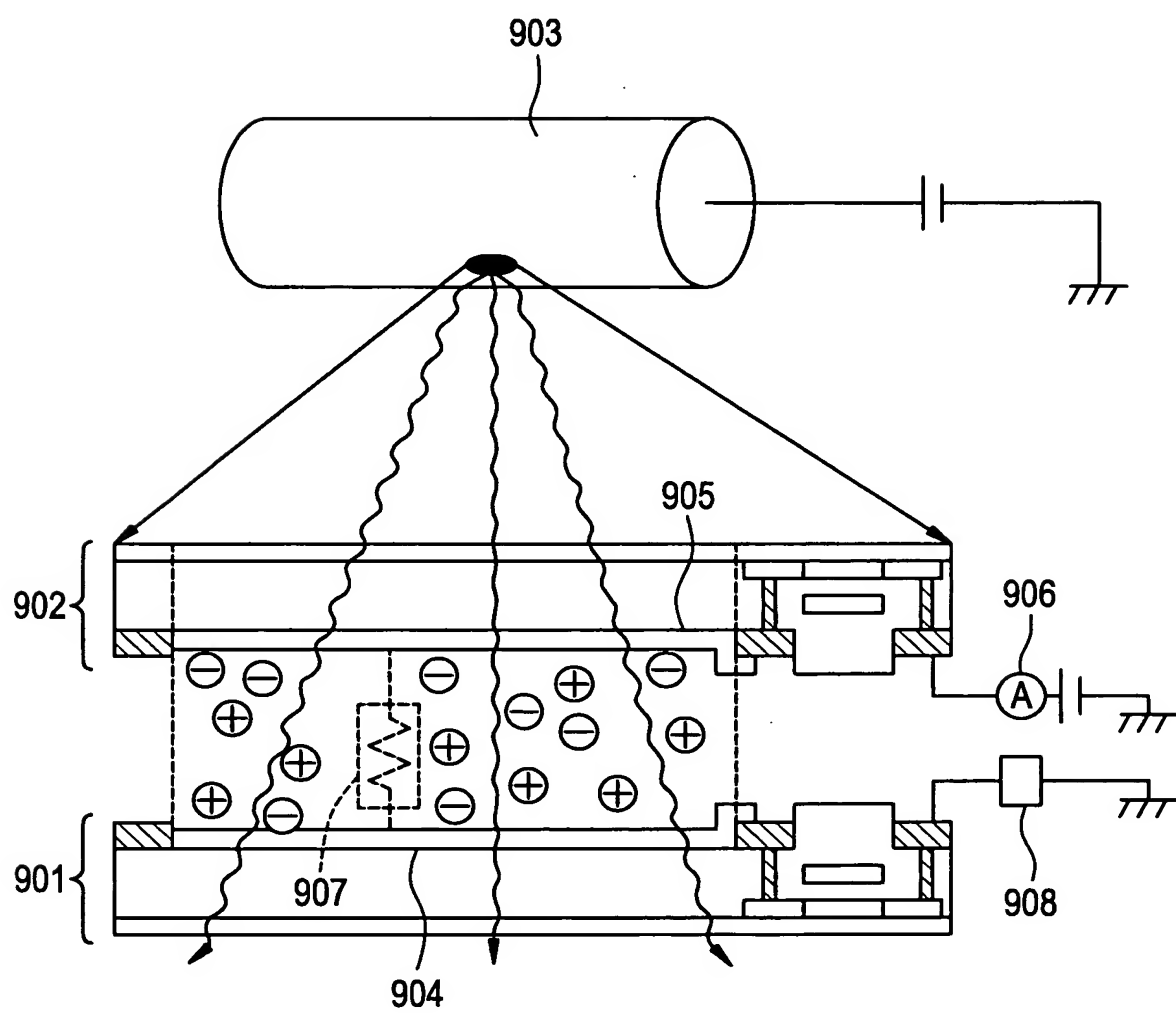


FIG. 10

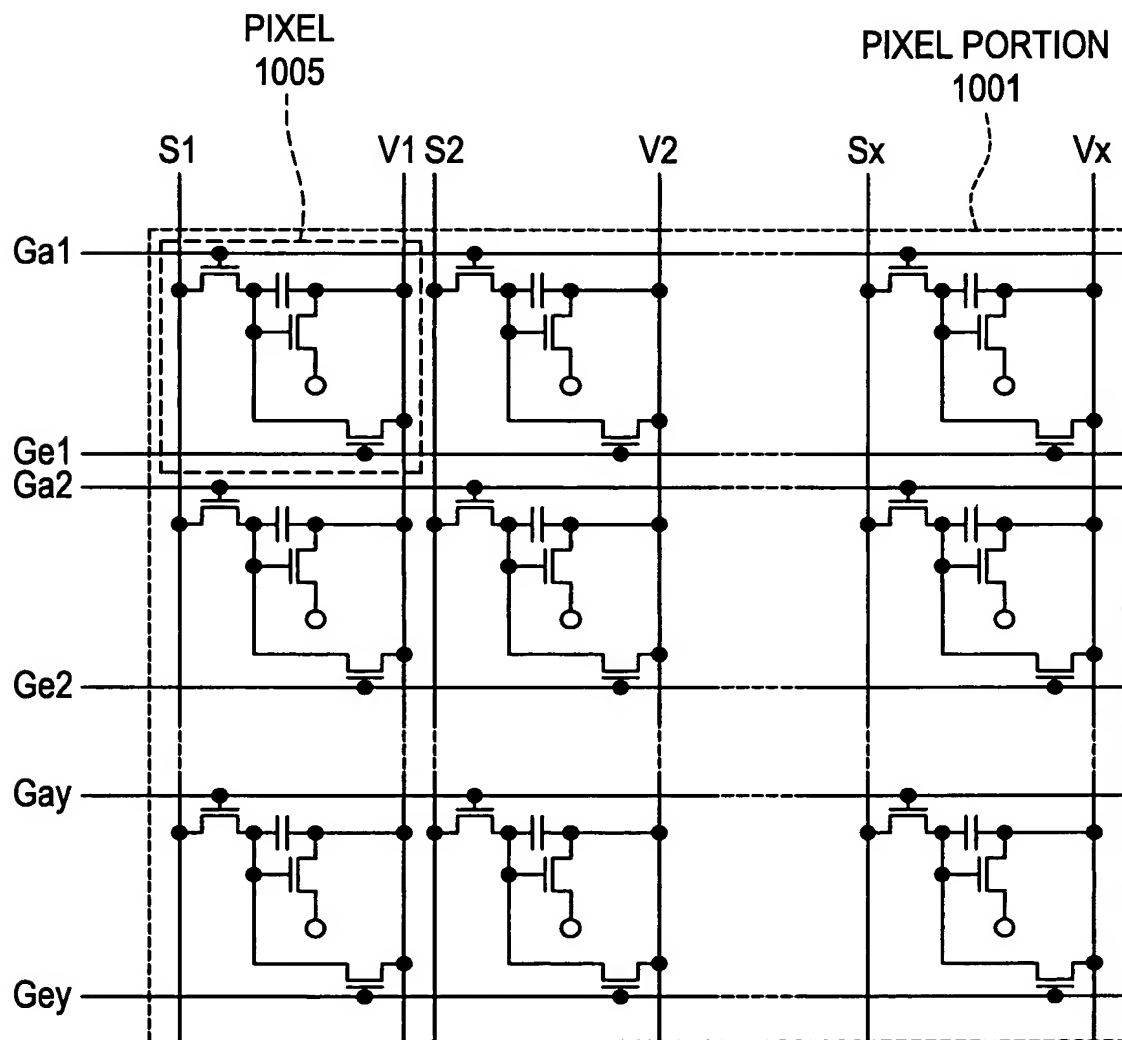


FIG. 11

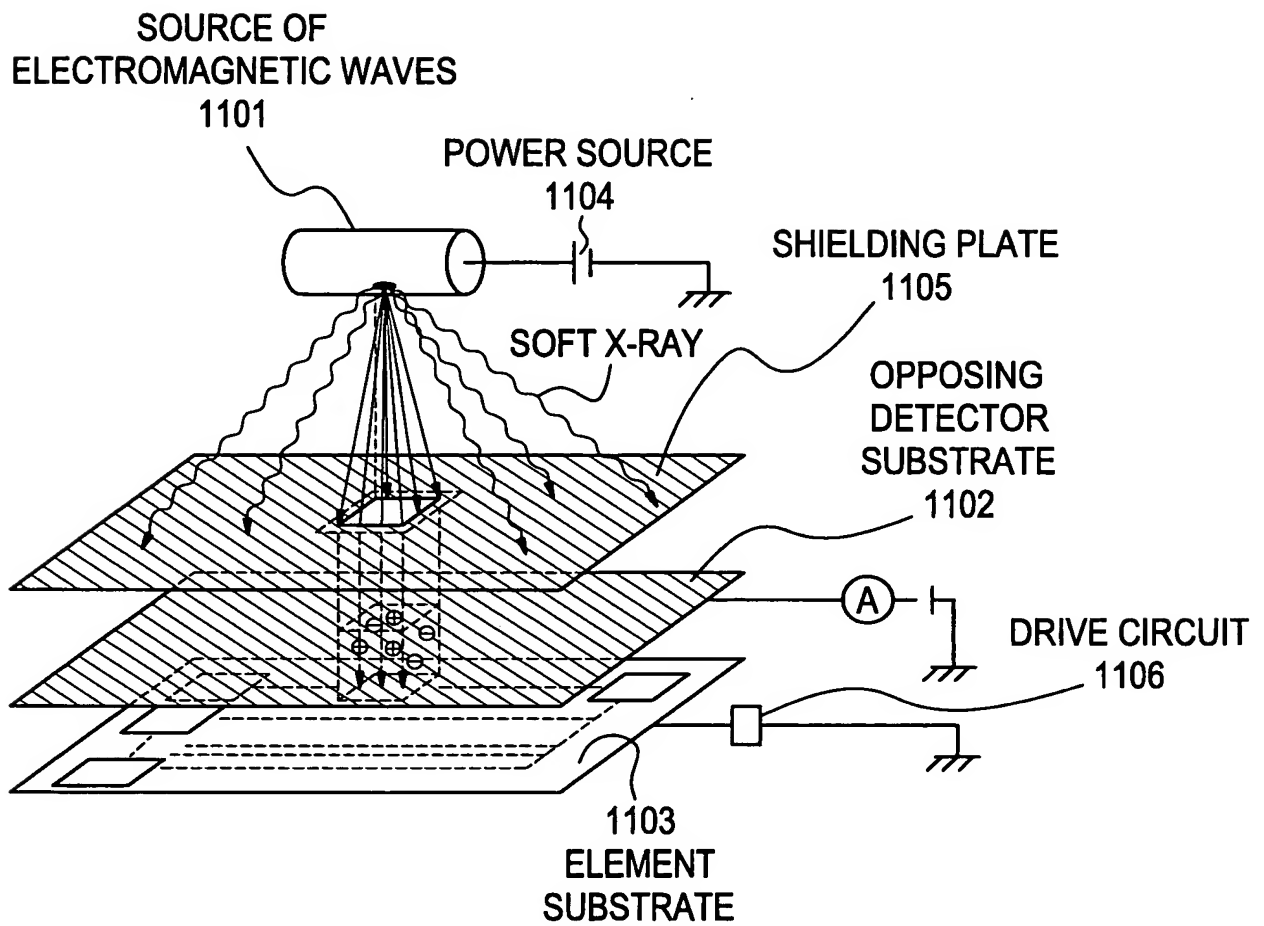


FIG. 12

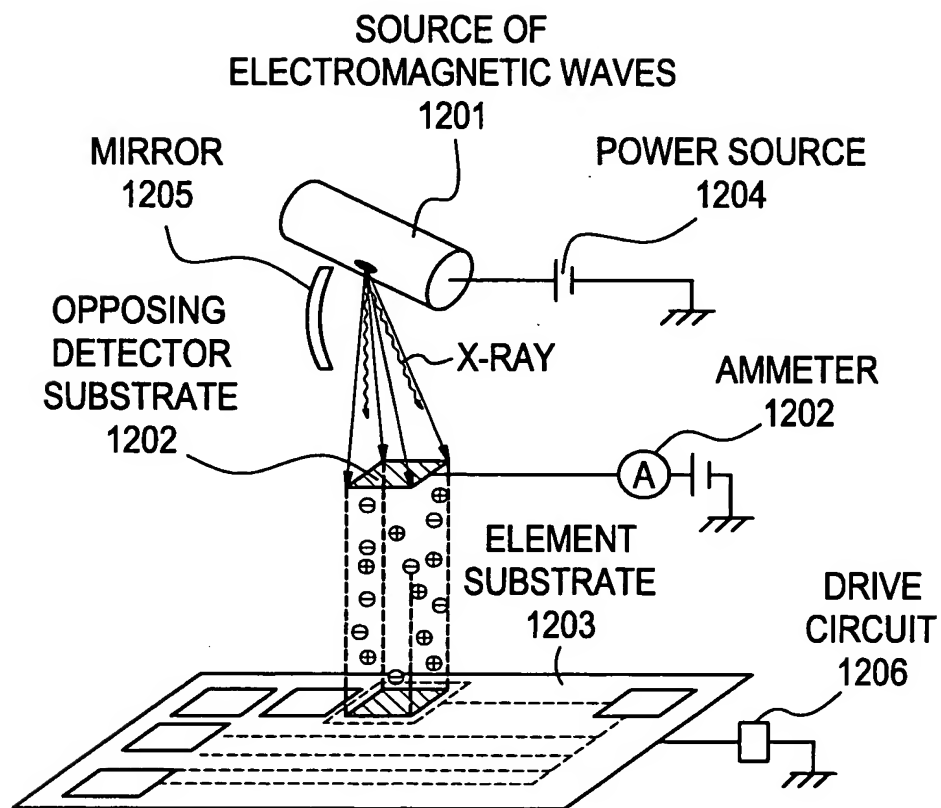


FIG. 13A

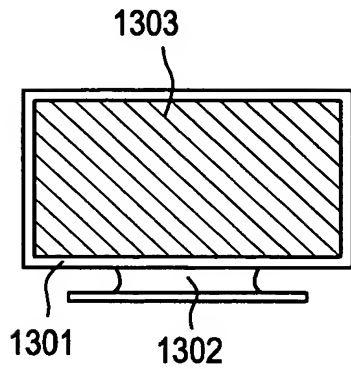


FIG. 13B

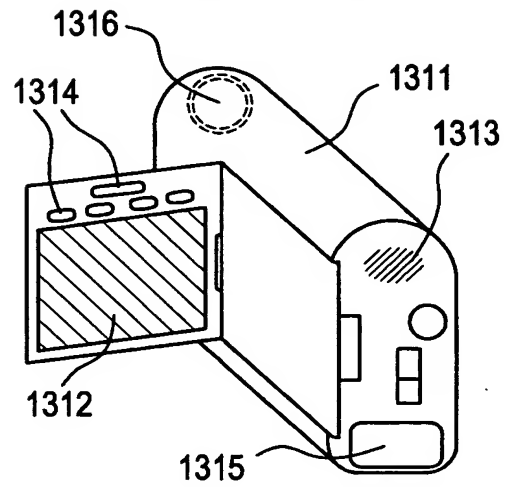


FIG. 13C

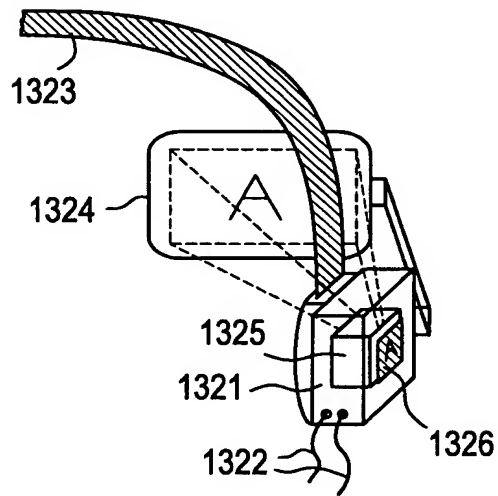


FIG. 13D

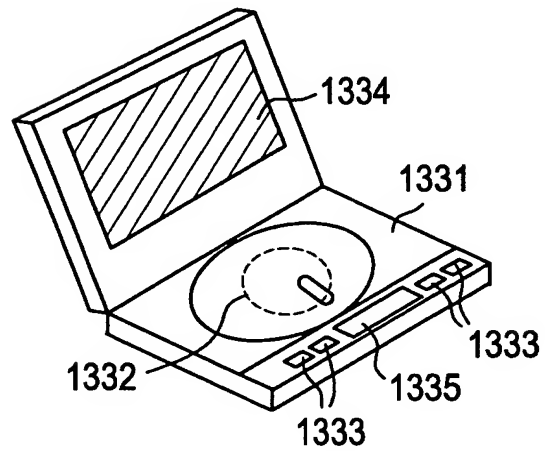


FIG. 13E

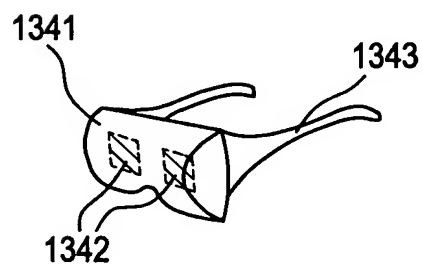


FIG. 13F

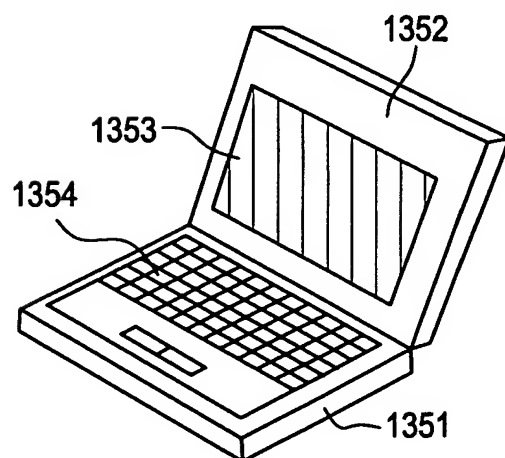


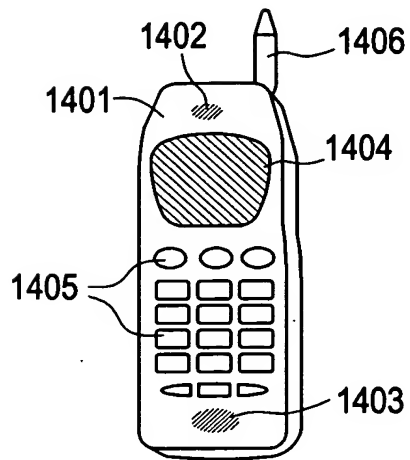
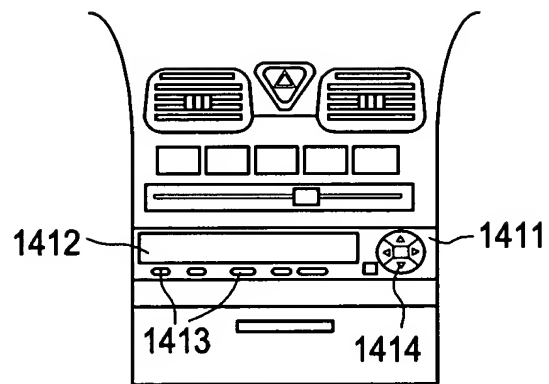
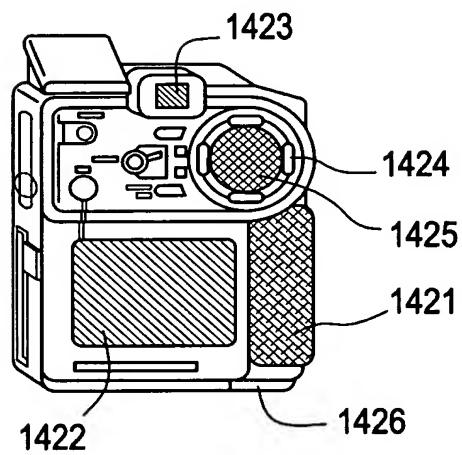
FIG. 14A**FIG. 14B****FIG. 14C**

FIG. 15

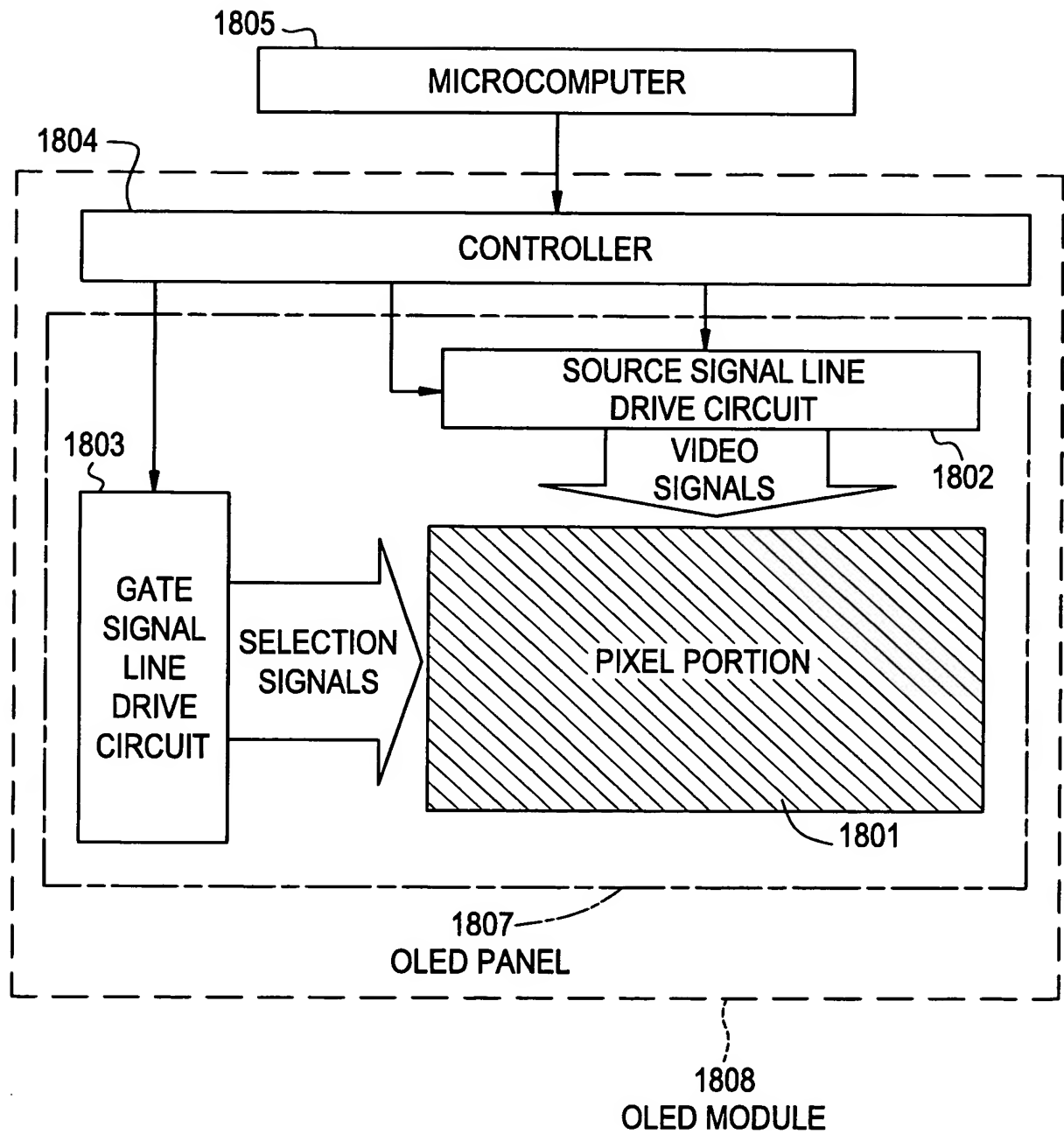


FIG. 16A

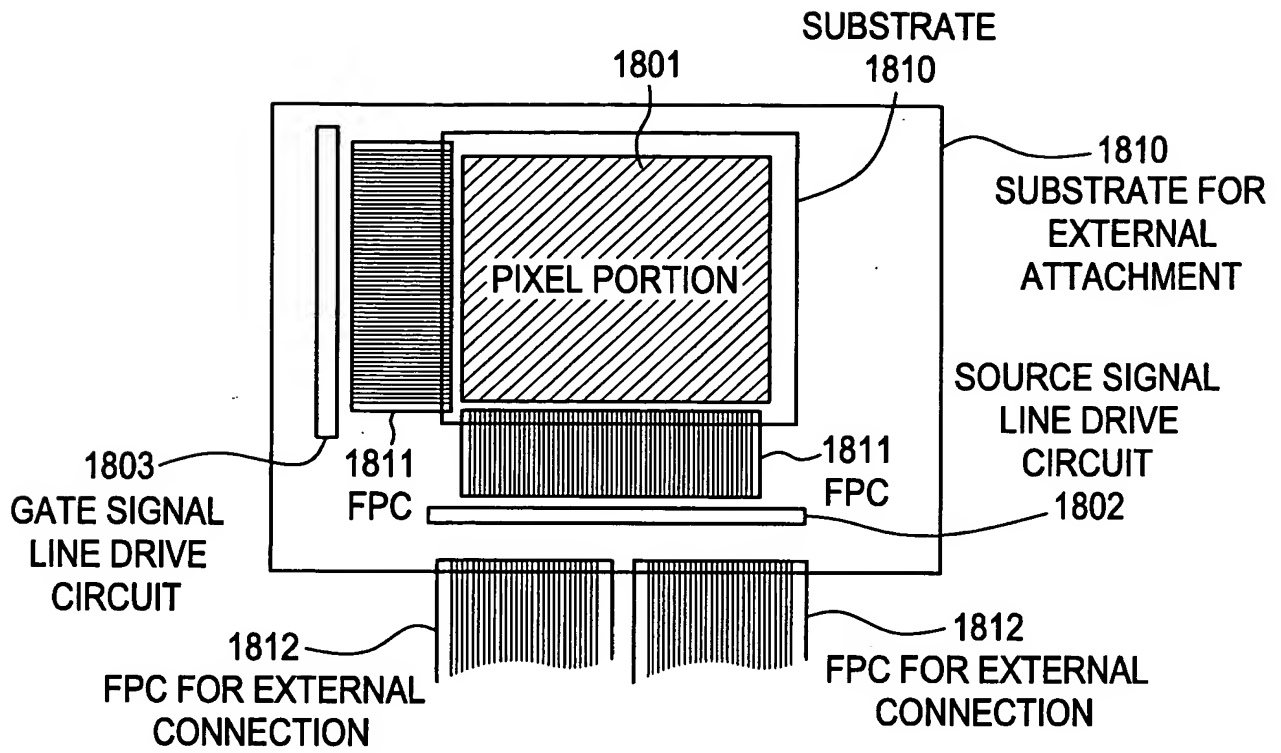


FIG. 16B

